# EEE4084F Quiz 2: Lectures 5-7 + Seminar 3

*This quiz is for marks!  27 Mar 2014*

***PLEASE ANSWER ON A SEPARATE PAGE***

***MAKE SURE YOUR STUDENT NUMBER IS ON YOUR ANSWER PAGE(s)***

**TOTAL NUMBER OF QUESTIONS :** FIVE

| # | Question | / | time (mins) |
|---|---|---|---|
| Q1 | The following questions related to memory access architectures…<br>(a) Explain what is meant when it is said that a mulicore processor system is cache coherent? [3 marks]<br>(b) Explain the acronym SMP [1 marks] and what can be said about how the memory access time varies for each processors in such a system [2 marks]. [total: 3 marks]<br>(c) Discuss two advantages and two disadvantages of shared memory. [4 marks] | 10 | 8.3 |
| Q2 | The following subquestion are based on programming heterogeneous parallel computers and parallel memory architectures.<br><br>Consider that a newly qualitifed computer engineer, Mr. Jobs, has been given the responsibility to implement a high-level parallel programming model for a heterogeneous parallel platform that consists of two multicore processor machines, both with graphics processing units (GPUs). However, one of the challenges Mr Jobs has is understanding how to map high-level algorithms to low-level executable patterns suitable for a GPU. Assists him by explaining to him (i.e., writing a written naration as answers to the below) the following...<br><br>(a) What type of machine according to Flynn's taxonomy is a GPU and why is it categorized as such. Because Mr Jobs is panicking a bit with his new job, state to him clearly what type of algorithms are suitable for a GPU. (you can use a rough diagram to assist your explanation.) [4 marks]<br>(b) Mr Jobs wants to run four parallel applications on the machines. Assume only one core in the one machine acquires the data and updates shared memory data accessible by the other cores on that machine. Discuss which type of parallel computer memory architecture is suitable for this application, and what sort of limitations and constaints might need to be considered (in terms of data transfer and processing) so as to effectively distribute the workload. [8 marks] | 12 | 10.0 |
| Q3 | **These question relates to Seminar 3.**<br>(a) What is meant by the term "Bisection Bandwidth"? You are welcome to provide a rough illustration if it helps your discussion. [6 marks]<br>(b) Contrast the most common differences between the back-end and front-end computing components of a HPEC system. You should be able to contrast three criteria for each. [3 x 2 marks = 6 marks] | 12 | 10.0 |
| Q4 | (a) Generally speaking, there tend to be eight steps involved in designing parallel programs. State three of these steps in the correct order they are usually carried out (i.e. where the frist step comes before the second, which comes before the third). [3 marks]<br>(b) In terms of converting a sequential program (with the source code available) to parallel version, provide some generalizations about where the engineering time tends to be focused on such a project. [4 marks]<br>(c) What is the difference between functional decomposition and domain decomposition? [3 marks] | 10 | 8.3 |
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| Q5 | (a) Explain the difference between synchronous and asynchronous communication. [4 marks]<br>(b) What was the LVDC? Briefly write in your own words why this, as well as the other computing systems developed for the Apollo missions, had a significant impact on the progress of computing systems. (Note: You are not expected to remember what the LVDC stands for, but you hopefully know where it was used and why it was needed). [6 marks] | 10 | 8.3 |
| Q6 | *Optional Extra Question for a bonus mark:*<br>What was the amount of RAM that came with the Altair 8800 MITS? (if you were listening in Seminar 3 you'd know the answer!)<br>(i) <=64 bytes (ii) 128 bytes (iii) 256 bytes (iv) 512 bytes (v) 1 Kbytes (vi) 2 Kb | +1 | |
| | **TOTAL :** | 54 | 45.0 |

*You can use this space for rough work if you like:*