Quiz 3: Lectures 8 and 9

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Instructions:

- Answer on a separate page.
- Make sure that your student number is on all your answer pages.
- There are 6 questions, each divided into sub-questions. Answer all questions.
- Total time: 45 minutes.
- Total marks: 50.

Question 1: Latency and Bandwidth [6 Total]

#1 Calculate the effective bandwidth for sending a message from one node to another in the following situation:

• Message size	1 024 bytes
• Speed of propagation	200 Mm/s
• Distance of copper cabling between nodes	200 m
• Raw bandwidth supported by the communication channel	50 Mbit/s
• Sending overhead	100 µs
• Receiving overhead	100 µs

Hint: remember Effective bandwidth = Message size / total latency **[6]**

Question 2: Communication [6 Total]

#1 Explain what is meant by a ‘barrier’ when referring to synchronisation. **[3]**

#2 Describe the difference between ‘broadcast’ and ‘scatter’ communication schemes. **[3]**

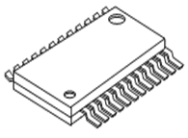
Question 3: Cloud Computing [7 Total]

#1 Briefly explain what is meant by ‘platform as a service’. **[3]**

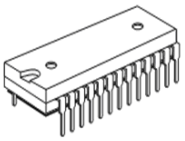
#2 With regards to cloud computing, what is meant by ‘virtualisation’. **[4]**

Question 4: Seminar Related Multiple Choice **[8 Total]**

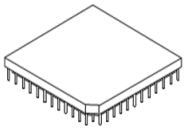
#1 Which of the following package types is a THT DIL (aka DIP) package? Select one of the letters for your answer below. **[2]**



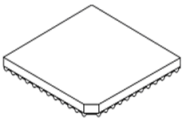
(a)



(b)



(c)



(d)

#2 In terms of chip testing based on running input tests on an n-input chip: the chip under test is considered fault-free if and only if which of one of the following conditions is met? (choose one answer only) **[2]**

a) It returns output true for any input given

b) All of its 2^n input patterns are handled correctly

c) If the output changes after the input is changed

d) If there is an input sequence that causes the chip to stop responding to inputs

#3 Answer 'ASIC' or 'FPGA' in response to each of the four statements below. Indicate whether an ASIC or an FPGA is relevant to the situation mentioned. **[4]**

1. This technology is reprogrammable
2. This technology is the faster of the two
3. This technology wastes very little space
4. This technology is more common for low-volume production

Question 5: GPGPU **[7 Total]**

#1 Describe, with diagrams, the OpenCL memory model. **[5]**

#2 By means of an example, explain the `get_global_id()` function and how to use it (from the kernel's point of view). **[2]**

Question 6: FPGA and ASIC **[16 Total]**

#1 What is meant by a 'cell' when referring to ASICs? **[2]**

#2 Draw a diagram of a typical FPGA logic unit. Hint: it's only 4 marks, so draw a simplified version **[4]**

#3 By referring to your diagram above, explain how a logic unit can be configured into an `and` gate. **[2]**

#4 Describe, with diagrams, a typical FPGA architecture. How are the logic units interconnected? How are these connections made reconfigurable? **[6]**

#5 Modern FPGAs have more than just reconfigurable logic units. Give two examples of these 'extra' features. **[2]**