EEE4084F Quiz 4: Lecture 17-19 + Seminar 9 (HPEC Trends)

This quiz is for marks! 15 May 2014

PLEASE ANSWER ON A SEPARATE PAGE

MAKE SURE YOUR STUDENT NUMBER IS ON YOUR ANSWER PAGE(s)

TOTAL NUMBER OF QUESTIONS : FIVE

#	Question	/	time (mins)
Q1	Answer the following multiple choice and Y/N questions (2 marks each): (i) In terms of the Cell Processor design, which one of these options correctly defines the SPE acronym? (a) Synthetic Processor Element (b) Systematic Process Evolution (c) Synthesizable Processing Element (d) Synergistic Processing Element (e) System Processor Entity (ii) Answer Y (Yes) or N (No) for the following: A BCE represents a single processing core in a multicore processor design, is used as an abstraction & simplification method for analysing performance of mutlicore architecture. (iii) Answer Y (Yes) or N (No) for the following: The PAM large RC system was constructed using single block of SRAM shared by an array of eight FPGAs. (iv) Answer Y (Yes) or N (No) for the following: Cray Research, well known for developing multiprocessor based supercomputers, also experimented with an FPGA-based reconfigurable platform built using Xilinx FPGAs.	8	9.0
Q2	Explain briefly, with a rough block diagram, how the input/output architecture is designed on the cell processor. Indicate how an SPE would perform IO (showing in particular if it needs to go via the PPU or otherwise).	8	9.0
Q3	(i) What does the acronym ABI stand for, in consideration of using this term in relation to program development as covered in the lectures. [1 mark] (ii) What does an ABI provide? Provide motivation for why an ABI can provide improved modularity and flexibility instead of simply providing all these solutions and specifications within an API (i.e., application programming interface). [6 marks] (iii) Name one of the APIs available for the Cell Processor. [1 mark]	8	9.0
Q4	A number of custom programming models have been described for the Cell Processor. These include: 1) Application-specific accelerators; 2) Function offloading; 3) Computation acceleration; and 4) Heterogeneous multi-threading (i) Select one of the programming models and provide a description of this programming model including a rough diagram to illustrate your explanation. [6 marks] (ii) Provide a short sentence or two motivation for why the developers decided to pose custom programming models such as these instead of simply sticking to the standard ones (e.g. divide and conquer) or a good-for-anything Round Robin type scheduling approach. [2 marks]	8	9.0
Q5	The formula on the right expresses Amdhal's Law: $\text{Speedup}_{\text{parallel}} = \frac{1}{(1-f) + \frac{f}{n}}$ (i) Explain what the parameters f and n represent. [2 marks] (ii) How would you experimentally determine the value of f? [2 marks] (iii) Is this function more likely a worst case performance prediction for a fine grained or for a course gained problem? Give a clear explanation to motivate your answer. [4 marks]	8	9.0
Q6	In Seminar 9 the SOA acronym was used a lot. What does SOA actually stand for? Choose one: (a) System Of Applications (b) Service Oriented Architecture (c) Sequence Of Application (d) Standard Order Applications (e) Semi Organized Arrangement	1	0
	TOTAL :	40	45.0