C to HDL Example

C CODE

```
/* 4-bit up-counter
 with reset alert. */
int count  = 0;
// this function runs
// all the time:
int upcount (
 _in int 4 data,
 _in int 4 target,
 _in bit loadcnt,
 _in bit reset,
 _out bit reset_alert )
{
 if (reset) count=0;
 if (loadcnt) {
    count=data;
    return 0; }
 count=(count + 1)%15;
 if (count==target)
    reset_alert=1;
 else reset_alert=0;
}
```

VHDL CODE

```
ENTITY upcount IS PORT(
  Clock: IN BIT; data: IN BIT_VECTOR (3 DOWNTO 0);
  target: IN BIT_VECTOR (3 DOWNTO 0);
  loadcnt, reset : IN BIT;
  reset_alert: OUT BIT );
END counter_4;

ARCHITECTURE behavioral OF counter_4 IS
BEGIN
 upcount: PROCESS( clock )
  VARIABLE count: BIT_VECTOR(3 DOWNTO 0);
 BEGIN
  IF (clock= '1') THEN
   IF (reset = '1') THEN
      count <= "0000";
   ELSIF (loadcnt='1') THEN count <= data;
   ELSE  -- full adder --
     count(0) <= NOT count(0);
     count(1) <= count(0) XOR count(1);
     count(2) <= (count(0) AND count(1)) XOR count(2);
     count(3) <= ( count(0) AND count(1) AND count(2) ) XOR count(3);
     IF count = target THEN
        reset_alert <= '1';
     ELSE
        reset_alert <= '0';
     END IF; -- IF count = target
   END IF; -- IF reset = ‘1’
  END IF; -- IF clock = '1’
 END PROCESS upcount;
END behavioral;
```