Accelerating a Software Correlator with High Performance Reconfigurable Computing

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Introduction

This project will investigate the performance gained, when using high performance reconfigurable hardware to implement the DiFX correlator, a software radio astronomy correlator.

What is Reconfigurable Computing (RC)?

Field Programmable Gate Arrays (FPGAs) are a type of hardware technology that is able to be 'rewired' to suit the task at hand. The amount of logic blocks available in a single FPGA is rapidly increasing as a result of new semiconductor fabrication techniques. FPGAs have reached a stage where huge, highly parallel, algorithms can be implemented entirely in FPGA logic. Reconfigurable computing is an approach that uses FPGAs as a co-processor in conjunction with a traditional microprocessor connected via high speed bus. The result is a system that is immediately compatible with legacy code but with the ability to greatly accelerate computationally expensive sections. RC has generated both academic and commercial interest and promises to have an exciting future in the high performance computing realm.

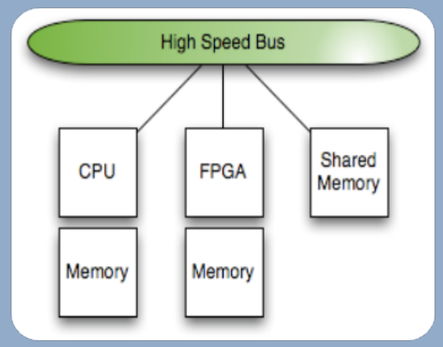

Figure 1: Diagrammatic representation of HPRC

Reconfigurable Computing (RC) Tooling

RC also aims to provide the RC developer with tools which resemble traditional software development. Programming an RC card often resembles ANSI C code, creating a more familiar environment to HPC users and appealing to a greater user audience. Although these tools still require a basic knowledge of the underlying hardware, it is a very new field and with more time could become the standard approach to hardware design.

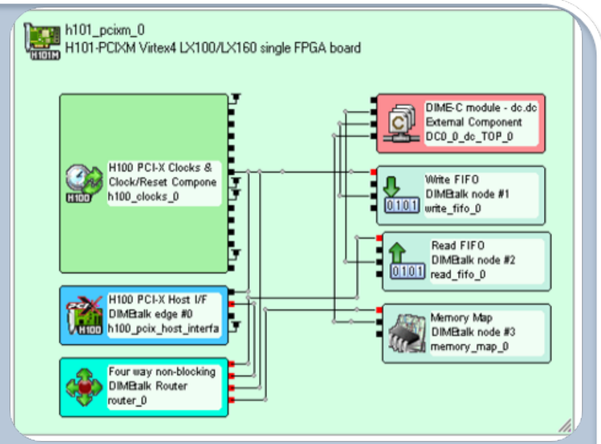

Figure 2: Example of a Dime-Talk Network from Nallatech

What is a Radio Astronomy Correlator?

Modern day large radio telescopes consist of a number of individual antenna which are used to detect electro magnetic radiation from interstellar objects. Alone, each of these antennas only produces very low resolution results. However if these individual antennas communicate, the collection of the received power can be combined, producing much richer results. The process of combining the individual received signals from each of the antennas, is the correlator's duty. As the number of antennas used increases, the amount of computation required grows rapidly.

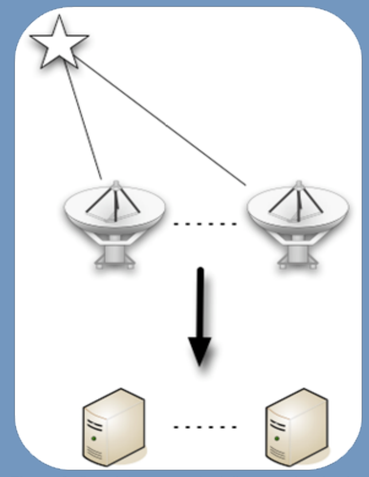

Figure 3: Correlator conceptual diagram showing large telescope array and huge computing clusters for processing.

Key Objectives of Project

An existing open source software correlator, DiFX, built for the Australian VLA is available. This correlator will be modified to meet Karoo Array Telescope (KAT) requirements. The modified DiFX correlator will provide a working correlator, which will potentially be used for the Production Equivalent Design (PED) telescope array and provide useful testing information for KAT correlator design.

HPRC is a new approach and few large projects have used it extensively. So it follows that there is little documented information on the experiences and problems faced with HPRC implementations. This project hopes to make a positive contribution to the information available and to provide a clearer indication whether HPRC is suitable for future KAT development.

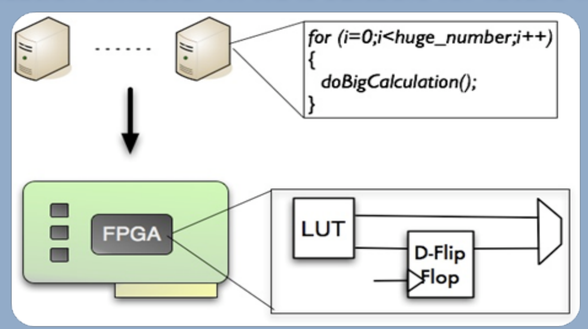

Figure 4: Correlator conceptual diagram showing the conversion of software running on traditional computers to hardware circuits in FPGAs.